REMARKS

Claims 62-95 are pending in the present application. In the Office Action dated June 27, 2005, claims 62-65, 68-75 and 78-82 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,186,670 to Doan et al. ("Doan") and in view of U.S. Patent No. 5,458,518 to Lee ("Lee"). Claims 66 and 76 were rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Lee as applied to claim 1 above, and further in view of U.S. Patent No. 5,869,169 to Jones ("Jones"). Claims 67, 77 and 83 were rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Lee and Jones as applied to claim 8 above, and further in view of U.S. Patent No. 5,793,154 to Itoh et al. ("Itoh"). Claims 84-88 and 90 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,473,222 to Thoeny et al. ("Thoeny") in view of Doan and Lee. Claim 89 was rejected under 35 U.S.C. 103(a) as being unpatentable over Thoeny, Doan and Lee and further in view of Jones and Itoh as in claim 67. Claims 62, 71-80 and 84-86 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1, 4-5, 7-9, and 45-46 of U.S. Patent No. 6,710,538.

The disclosed embodiments of the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

One embodiment disclosed in the present application includes a field emission display having a substrate and a plurality of emitters formed on the substrate. Each of the emitters is formed on one of a plurality of emitter conductors that is also a row or a column of the display. The display includes a porous silicon dioxide dielectric layer that is formed on, disposed over, and bonded to an upper surface of the substrate and the columns. Thus, the porous silicon dioxide dielectric layer is a separate, distinct layer from the substrate and is located physically above its underlying substrate. In one embodiment, the porous silicon dioxide dielectric layer is planarized by a process such a chemical-mechanical polishing or mechanical polishing to form a mechanically planarized upper surface. The porous silicon dioxide dielectric layer has an opening formed about each of the emitters and has a thickness substantially equal to a height of the emitters above the substrate. The porous silicon dioxide dielectric layer may be formed by oxidation of porous polycrystalline silicon. The display further includes an extraction grid formed substantially in a plane defined by respective tips of the plurality of emitters. The

extraction grid has an opening surrounding each tip of a respective one of the emitters. The display additionally includes a cathodoluminescent-coated faceplate having a planar surface formed parallel to and near the plane of tips of the plurality of emitters.

The examiner has Doan, which discloses a field emission device having a silicon dioxide insulating layer formed on a substrate. However, Doan fails to disclose using porous silicon dioxide. If any teaching is present in Doan with regard to varying the dielectric properties of the insulating layer 14 (*i.e.* , the silicon dioxide layer), it would be modifying the chemical composition of the insulating layer 14 and not its microstructure to control the dielectric properties. (Doan, col. 5, lines 6-14). For example, Doan suggests using a variety of different compositions (*i.e.*, using silicon dioxide, silicon nitride, or silicon oxynitride) and does not mention altering the microstructure of the material layer 14 (*e.g.*, porosity) to alter its dielectric properties. (Doan, col. 5, lines 6-14).

The examiner has also cited Lee. Lee discloses a method of fabricating emitter arrays and the resulting emitter array structure. One major problem that Lee seeks to solve is the purported lower quality of silicon dioxide layers formed by depositing the silicon dioxide using electron beam evaporation, which are taught to be of lower quality and difficult to control repeatability. (Lee, col. 2, lines 2-7). For example, such a silicon dioxide layer is shown in Doan as the layer 14. Lee solves the above problems by forming a porous silicon dioxide layer within the substrate. The porous silicon dioxide layer is formed by etching a silicon substrate 10 to a predetermined depth of about 1 μm by etching in hydrofluoric acid with an electric current applied to form a porous silicon layer 12 in the substrate 10. The porous silicon layer 12 is subsequently oxidized at a temperature of, for example, 1000 °C to form a porous silicon dioxide layer 24. Thus, in contrast to Applicants' embodiments where the porous silicon dioxide layer is located on and physically above the substrate, the porous silicon dioxide layer 24 of Lee is physically located within the substrate 10.

Lee clearly teaches away from providing a porous silicon dioxide layer on and physically above the substrate 10 because it criticizes the purported difficulty in obtaining consistent process conditions when a silicon dioxide layer is deposited on the substrate 10. In other words, Lee clearly teaches away from providing a porous silicon dioxide layer that is bonded to an upper surface of an underlying substrate and, thus, located physically above its underlying substrate. Lee provides a porous silicon dioxide layer 24 by integrally forming the

layer from the substrate 10 and such a layer clearly is not bonded to an upper surface of the substrate. Instead, the porous silicon dioxide layer 24 defines a portion of the substrate.

The combination of Doan and Lee would result in a field emission display baseplate in which the silicon dioxide layer 14 is provided within and physically located within the silicon substrate 11 of Doan. Thus, unlike Applicants' embodiments, the combination of Doan and Lee does not result in a field emission display baseplate in which a porous silicon dioxide layer is disposed over and bonded to an upper surface of its underlying substrate. The combination of Doan and Lee does not teach or suggest a field emission display baseplate having a porous silicon dioxide layer that is located and positioned as shown and described in Applicants' embodiments. The other cited references do not remedy any of the above deficiencies of Doan and Lee.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Claim 62 recites, in-part, "a porous silicon dioxide layer including respective openings coaxial with the emitter bodies, the porous silicon dioxide layer disposed over and bonded to the upper surface of the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being disposed over and bonded to an upper surface of the substrate. In particular, the combination of Lee and Doan does not teach or suggest the structure of the dielectric layer and its corresponding position relative to the substrate.

Claim 68 recites, in-part, "an oxidized porous polysilicon layer disposed over and bonded to the upper surface of the substrate and the conductors." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being disposed over and bonded to an upper surface of the substrate. In particular, the combination of Lee and Doan does not teach or suggest the structure of the dielectric layer and its corresponding position relative to the substrate.

Claim 71 recites, in-part, "an oxidized porous polysilicon layer disposed over and bonded to the upper_surface of the substrate and of the conductors." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being disposed over and bonded to an upper surface of the substrate. In particular, the combination of

Lee and Doan does not teach or suggest the structure of the dielectric layer and its corresponding position relative to the substrate.

Claim 78 recites, in-part, "a porous silicon dioxide layer disposed over and bonded to the upper surface of the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three, the porous silicon dioxide layer including respective openings formed about each of the emitters." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being disposed over and bonded to an upper surface of the substrate. In particular, the combination of Lee and Doan does not teach or suggest the structure of the dielectric layer and its corresponding position relative to the substrate.

Claim 84 recites, in-part, "a porous silicon dioxide layer including respective openings formed about each of the emitter bodies, the porous silicon dioxide layer disposed over and bonded to the upper surface of the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being disposed over and bonded to an upper surface of the substrate. In particular, the combination of Lee and Doan does not teach or suggest the structure of the dielectric layer and its corresponding position relative to the substrate.

Claims depending from claim 62, 68, 71, 78, and 84 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, dependent claims 91-95 each contain limitations directed to a porous silicon dioxide layer or an oxidized porous polysilicon layer that has a mechanically planarized upper surface. The Examiner has cited Lee for disclosing a porous silicon dioxide layer having a planarized upper surface. However, to the extent that of Lee even discloses a planarized upper surface, the planarized upper surface is an etched planarized upper surface. Accordingly, Lee fails to disclose or fairly suggest a porous silicon dioxide layer having a mechanically planarized upper surface and the inherent structural differences associated with a mechanically planarized surface as opposed to an etched planarized surface. It is also noted that limitations such as "mechanically planarized" have been construed as limiting the structure of a claimed product and, thus, must be given patentable weight as a structural limitation. See, M.P.E.P. § 2113 (citing In re Garnero, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979)(holding "interbonded by interfusion" to limit structure of the claimed composite and

noting that terms such as "welded," "intermixed," "ground in place," "press fitted," and "etched" are capable of construction as structural limitations). In other words, under the holding of In re Garnero, the limitation mechanically planarized is a structural limitation and should not be construed as a product-by-process limitation.

With regard to the obviousness-type double patenting rejection, Applicants are filing a terminal disclaimer to obviate it. Accordingly, the rejection of claims 62, 71-80, and 84-86 under the judicially created doctrine of obviousness-type double patenting should be withdrawn.

All of the claims remaining in the application (claims 62-95) are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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